4-8-02 PB

PATENT
Attorney Docket No. 401558/SAKAI

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAKAO HASEGAWA

Application No. Unassigned

Art Unit: Unassigned

Examiner: Unassigned

Filed: February 13, 2002

For: METHOD OF WIRING SEMICONDUCTOR INTEGRATED CIRCUIT, SEMICONDUCTOR INTEGRATED CIRCUIT, AND COMPUTER PRODUCT

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to the examination of the above-identified patent application, please enter the following amendments and consider the following remarks.

IN THE SPECIFICATION:

Replace the paragraph beginning at page 2, line 19 with:

a1

An insulation layer is disposed between the first layer and the second layer, thereby to insulate the wirings belonging to one layer from those of the other layer. It is necessary to electrically connect between the a-wiring 1 and the A-wiring 8, and between the a-wiring 2 and the A-wiring 8 respectively, as these wirings handle the same signal. For this purpose, the a-wiring 1 and the A-wiring 8 are connected to each other via the through-hole 5, and the a-wiring 2 and the A-wiring 8 are connected to each other via the through-hole 6. These through-holes are provided to pierce through the insulation layer sandwiched between the first layer and the second layer, in a direction perpendicular to the circuit surface, respectively. Therefore, it is possible to secure electric conduction between the first layer and the second layer through these through-holes. In order to provide these through-holes, according to a conventional automatic wiring, wiring patterns are set subject to a condition that one through-hole is disposed without exception to a pair of these wirings to be connected to each other. Specifically, in the automatic wiring, a setting area is provided on one of the